

Integrated Multi-input Bi-directional DC-DC Converter for Hybrid Energy Storage Systems

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Abstract—Multi-input bidirectional DC-DC converter is quite vital for a single system to interface multiple sources and allow energy exchange between sources and loads. In this paper, a general multi-input DC-DC converter topology and its control strategy are proposed for hybrid energy storage system. This converter can connect any number of power sources and make any ports controllable bidirectionally. To interface N power sources, only $N + 1$ controllable power switches are needed, which makes converter more compact with largely reduced power devices and driving circuits. Without loss of generality, a case with two sources ($N = 2$) is utilized as a typical study case for experimental verification. Experimental results show this converter can interface two individual power sources simultaneously and ensure flexible power flow control with all ports bi-directionally. $N = 2$ converter structure can be developed as an integrated converter module, which is able to combine with traditional bidirectional buck/boost DC-DC converter (BBDC) to construct series-connected or parallel connected integrated converters for multi-source applications.

Index Terms—Bidirectional, DC-DC converter, hybrid energy storage, integration, multi-input.

I. INTRODUCTION

FOR energy storage systems, many bidirectional power sources like batteries and supercapacitors are usually used for smoothing power flow between input and output under various load conditions. To ensure reliable power flow control, many different bidirectional DC-DC converters are utilized in renewable power systems, electric vehicles, and uninterruptible power supply applications [1]–[3]. Normally, to interface one power source, a single-input single-output (SISO) DC-DC

converter is required. To interface hybrid energy sources, the multiple SISO converters [4]–[15] or integrated multi-input DC-DC converters (MIC) [16]–[35] should be utilized. Generally, as compared with cases with N separate SISO converters, less power devices are needed in multi-input converter to connect N sources. Therefore, using the same number of switching devices, more power sources can be connected, and higher output power can be achieved. In addition, only a unified controller is required in MIC to ensure integrated power flow control, while several separated controllers should be involved in traditional multiple SISO system.

Most MICs are developed based on basic DC-DC converter topologies such as buck converter, boost converter, buck/boost converter, half bridge and full bridge converters, etc. [16]–[35]. MIC can be divided into two types: isolated and non-isolated ones. Several isolated-MICs have been proposed in [16]–[19]. In isolated-MICs, a multi-winding transformer is mandatorily required to ensure reliable isolation, bidirectional power transfer, and high ratio in voltage conversion. However, due to using isolated transformer, overall system volume and costs would be higher, and power density would be lower. Furthermore, some crucial issues such as core saturations, leakage inductance, and high spike voltage in power switches also exist in isolated MICs.

Due to compact structure, reduced component count, higher power density and fewer power conversion stages [20]–[35], the non-isolated MIC is also attractive. A general method to synthesize MICs with traditional buck and boost converters, buck/boost converters, etc., has been presented in [20]. These constructed MICs can ensure individually or simultaneously power supply for load. Different types of dual-input and three-input non-isolated MICs have been presented in [21]–[24]. In [21], to ensure high voltage boost ratio, a dual-input boost converter is proposed with five power switches and two coupled inductors. A dual-input boost converter with lowered power components is proposed in [22], in which only three switches and one coupled inductor are needed. In [23], a DC-DC boost converter with three input sources is proposed. In the converter, all power sources can be used to support load, and battery can also be charged by fuel cell and PV sources. A three-input boost converter with four power switches and diodes is proposed for connecting three different type of power sources in [24]. Some generalized MIC topologies are developed in [25]–[27]. In [25], a MIC boost converter with expandable input modules is proposed for PV system. In this converter, voltage boost ratio can be adjusted by changing turn ratios in the coupled inductor. A single-

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inductor MIMO converter based on series-connected input cells and output cells is proposed in [26]. In this topology, $2N$ power switches and diodes are required to interface N power sources. Although only one shared inductor is used, overall cost is still high. A soft-switched non-isolated multiport DC-DC converter with high boost ratio is proposed in [27]. This converter can ensure soft-switching, high boost ratio, and independent power flow control. However, this converter needs more power switches and coupled inductors. To be noted here, all the aforementioned non-isolated MICs are unable to ensure all port bidirectional.

Some non-isolated MICs with bidirectional power flow control capability have been discussed in [28]–[35]. In [28], three bidirectional buck/boost DC-DC converters (BBDC) are parallel connected to construct a bidirectional MIC. Similarly, in [29], a modular non-isolated multi-input DC-DC converter is proposed to achieve high boost ratio with reduced voltage stress. In this converter, all unit converter modules are parallel connected to a common DC-link. In [30], an interleaved DC-DC converter with two bidirectional input power sources is proposed, which can boost DC bus voltage individually or simultaneously, and also can buck DC-bus voltage to charge power sources. From the point of view of these topologies in [28]–[30], there is no difference with those multiple converters because all these converters utilize independent converter units to interface different power sources. In [31], a MIC that can operate in buck, boost or buck/boost modes is proposed. In this topology, all power sources can be interfaced with a common inductor. However, more power switches are required as compared with topology in [4]. In [32], for energy storage system applications in DC microgrid, a multi-input DC-DC converter is proposed with wider range of voltage conversion and lowered voltage stresses. However, to interface N power sources, $2N$ power switches are required. A dual input DC-DC converter with bridge-type structure is proposed in [33] to achieve high efficient integration of two bidirectional sources. However, this converter needs two IGBT with antiparallel-diodes and two IGBT without antiparallel-diodes, which is not easy for modular design. In addition, the two sources are not commonly grounded. In [34], a dual-input DC-DC boost converter with higher DC-bus voltage is proposed. This converter only needs three power switches, but output voltage should be higher than the sum voltage of the two sources. In [35], a compact dual-input DC-DC converter is proposed, which only uses three power switches to connect two bidirectional sources. However, general design and control method for synthesizing the MIC topology with arbitrary number of input DC sources is not developed.

In this paper, the main contribution is to develop a general integrated multi-input bidirectional DC-DC converter topology and its control strategies. This converter uses $N + 1$ series connected power switches and N inductor to interface N power sources. By using a unified energy control algorithm, the integrated power converter can function as N groups of bidirectional buck/boost converters. Basic features of the proposed converter are summarized as follows: 1) the converter can interface any number of input power sources; 2) all input ports and output port are bidirectional; 3) power flow from/to

sources can be controlled individually, which can make energy management of power sources more flexible; 4) converter is applicable to bidirectional DC-DC systems with minimal power switch counts. For verification, $N = 2$ based tri-port bidirectional DC-DC converter is selected as an example in experiments.

The article is organized as following sections: in Section II, operational principles and control strategies of proposed converter topology are analyzed; Section III discussed the study case with two sources; Experimental results are presented in Section IV, and a conclusion is drawn in Section V.

II. OPERATIONAL PRINCIPLE OF THE PROPOSED CONVERTER

A. Topology of the Integrated Multi-input Converter

To connect N power sources and ensure all ports bidirectional, a general multi-input integrated bidirectional DC-DC converter is proposed. Topologies derivation process is shown in Fig. 1. As shown in Fig. 1(a), traditional BBDC is used to interface one power sources. When source number $N = 2$, a three-switch leg-based converter is developed in Fig. 1(b). As compared with traditional BBDC topology, only one additional power switch is added. With respect to battery source 1, if S_{1a} and S_2 are deemed as a common switch S^* , $V_1-L_1-S_{1b}-S^*$ can construct an equivalent BBDC cell. Similarly, if S_2 and S_{1b} are deemed as one common switch $S^\#$, $V_2-L_2-S_{1a}-S^\#$ can construct second equivalent BBDC cell. Thus, if only one power switch is in OFF state at any time of an electric cycle, turn ON/OFF signals of upper and lower power switches of equivalent BBDC cells are always in complement. Thus, two BBDC cells can be controlled in a decoupled way.

When $N > 2$, generalized topology is illustrated in Fig. 1(c). As can be seen in this figure, there are N sources $V_1, V_2, \dots, V_N$ connected to a chain of $N+1$ switches through N filter inductors $L_1, L_2, \dots, L_N$. Output DC bus voltage is V_0 , which is higher than all input voltages. Loads of converter can be a bidirectional energy source, a resistor load, or a converter-based motor drive system. As can be seen in topology, in order to connect N power sources, only $N + 1$ power switches are required.

These switches are operated in pairs from $1, 2, \dots, n$, with n given by:

$$n = \left\lceil \frac{N+1}{2} \right\rceil \quad (1)$$

where $\lceil \cdot \rceil$ is ceiling function. If N is even, then the last pair will only have one switch S_n , instead of S_{na} and S_{nb} .

For each source, converter is operated as if all upper switches behave like one switch and all lower switches behave like one switch. Collectively, upper switches and lower switches are operated in a complementary way to form a buck/boost converter. In order to obtain ON state for upper (lower) switches corresponding to a source, then all upper (lower) switches should be turned ON; in order to obtain OFF state for lower (upper) switches, then only one switch needs to be turned OFF. Hence, it is possible to just have one switch (and only one) turned OFF at any time. By allocating which

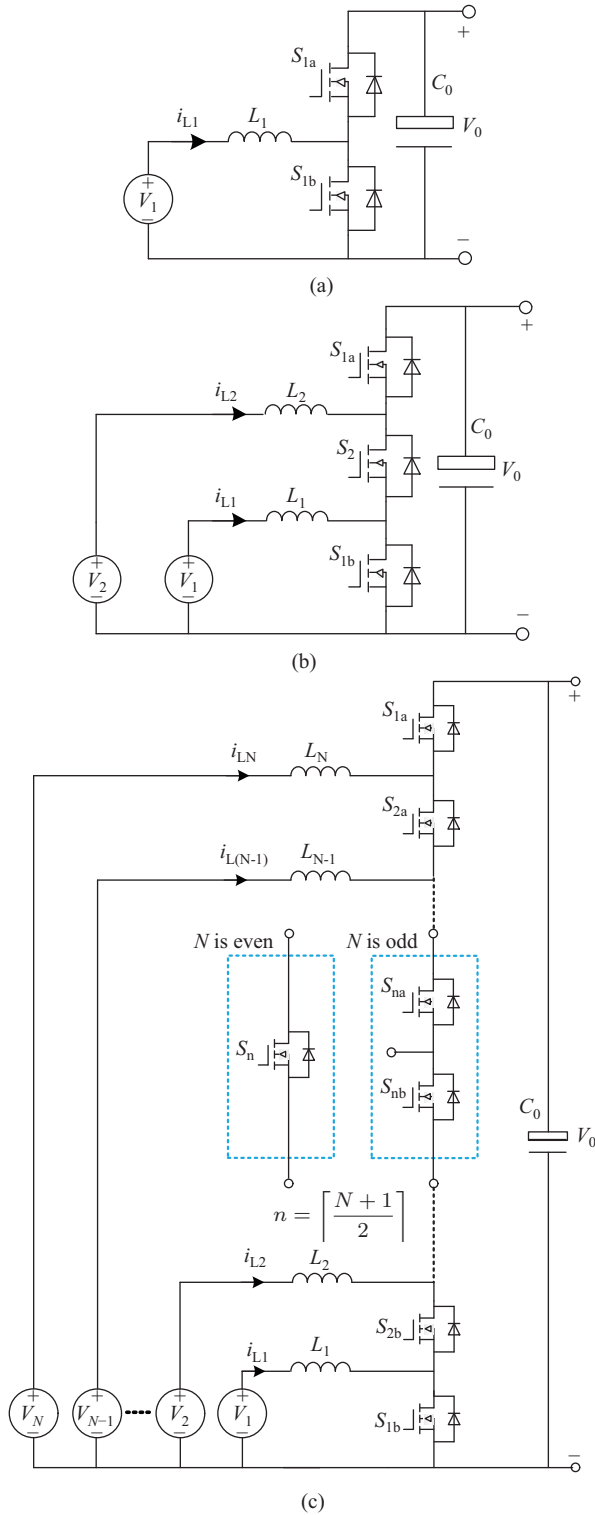


Fig. 1. Generalization of the integrated multi-input bidirectional DC-DC power converter. (a) Traditional BBDC converter with one power source. (b) Integrated DC-DC converter with two sources. (c) The multi-input DC-DC converter with N sources.

switch to be turned OFF, it is possible to charge/discharge all N sources. Counting output port V_0 together, the proposed converter has in total $N + 1$ bidirectional ports.

Taking h -th source V_h ($1 \leq h \leq N$) as an example, it is discharged to charge filter inductor L_h if all of switches $S_{1b} \sim$

S_{hb} are turned ON. If any switches $S_{1b} \sim S_{hb}$ are turned OFF, then stored energy in the inductor L_h flows to output V_0 . Because V_0 is higher than V_h , current flowing through inductor decreases, and if OFF state lasts long enough, inductor current crosses zero and starts charging source. Hence, operation is bidirectional for each source.

To be noted here, $N + 1$ power switches series connection topology can be easily constructed with two types of switch modules as in Fig. 2. Therefore, the proposed converter can meet requirements of modular design.

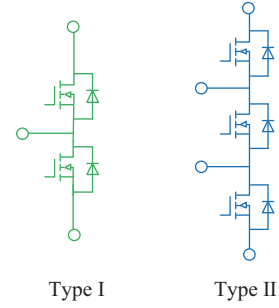


Fig. 2. Two types of the power switch modules.

B. Operational Principle and Control Strategy

Based on the energy conservation law, power released and absorbed by all ports should be equal when loss is negligible, i.e.

$$\sum_{i=1}^{N+1} P_i = 0 \quad (2)$$

where P_i is defined as positive when port sources power or negative when port sinks power. Port 0 corresponds to output port (DC bus).

To control power flow between sources and output (loads), two types of control algorithms can be developed according to load types.

1) *Control type I*: For loads like resistors, LED, DC-DC converter-based DC-load systems, and inverter-based motor drive systems, bus voltage V_0 needs to be controlled to track reference value V_{0ref} . One possible option is to adopt a Voltage Control Module (VCM) to regulate DC-bus voltage via controlling one source, e.g. source V_1 , as illustrated in Fig. 3(a). This is a voltage-current cascaded regulation loop and could be tuned with ease. As can be seen in Fig. 3(a), switching signal S_{1b} as represented by q_{1b} can be obtained

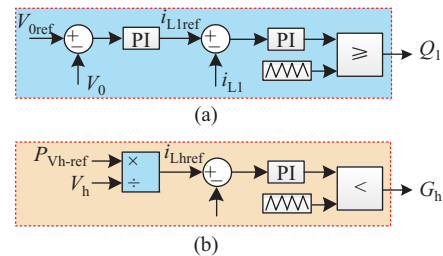


Fig. 3. Control modules needed for converter with more than 2 sources ($N > 2$). (a) Voltage control module VCM. (b) Power control module PCM_h.

via the VCM. Other ports can be controlled to regulate power exchanged, through Power Control Modules (PCM) shown in Fig. 3(b). This is in principle a current tracking controller, after converting reference power into reference current. According to energy conservation law, supported and consumed energy should be equal without considering loss. In this case, once power reference of input power sources $V_2 - V_N$ are preset, power flow can be handled by power source V_1 .

2) *Control type II*: For loads like battery banks, super capacitors, and other bidirectional power source or energy storage systems, DC-bus voltage could be restricted naturally by load. In this case, all source port can be controlled to regulate power exchange through the PCM shown in Fig. 3(b). Thus, once reference power of input power sources are preset, power flow of system can be handled directly by loaded power sources. Corresponding logics between switching signals and input power sources in PCM control modules are shown in Table I. As illustrated in this table, according to parity of source number, the relationship between order number of power sources and order number of switches shown in Fig. 1(c) can be determined. Thus, drive signals of related switches in proposed converter topology can be generated by the PCM module as illustrated in Fig. 3(b).

TABLE I
THE CORRESPONDING LOGICS BETWEEN SWITCHING SIGNALS AND
INPUT POWER SOURCES IN THE PCM AS SHOWN IN FIG. 3(B)

Parity of N	Value range of h	Relationship between k and h	Corresponding switch logics
N is odd	$1 \leq h \leq 0.5(N+1)$	$k = h$	$G_h = \bar{q}_{kb}$
	$0.5(N+1) \leq h \leq N$	$k = N+1-h$	$G_h = q_{ka}$
N is even	$1 \leq h \leq 0.5N$	$k = h$	$G_h = \bar{q}_{kb}$
	$0.5N+1 \leq h \leq N$	$k = N+1-h$	$G_h = q_{ka}$

Note: N is the number of the power sources, h means the h^{th} power sources, G_h is the generated switching signal of the h^{th} PCM, q_{ka} and q_{kb} are the switching signals of the power switches S_{ka} and S_{kb} ($1 \leq k \leq n$), respectively.

The challenge lies in how to determine gate drive signals for all switches. This is discussed separately for three cases:

1) When $N = 1$, converter is a conventional two-quadrant buck/boost converter. In control type I, as presented in Fig. 4(a), gate signals of upper/lower power switches can be generated by applying the VCM shown in Fig. 3(a) to switch S_{1b} , denoted as VCM_1 . Gate signal for switch S_{1a} is complementary to S_{1b} . It is clear bus voltage can be easily regulated to track reference value. In control type II, the VCM_1 module can be replaced by PCM_1 with a NOT gate cascaded.

2) When $N = 2$, converter is regarded as two buck/boost DC-DC converter cells. Only one power switch is turned OFF at any time. Overall operational logic block diagram for control type I and II are presented in Fig. 4(b). In control type I, operation of Switch S_{1b} remains the same as the case with $N = 1$ to regulate DC bus voltage through VCM_1 . Instead of operating S_{1a} to be exactly complementary to S_{1b} , it is operated through a power control module PCM_1 so power could be controlled, as shown in Fig. 4(b). Additional switch S_2 should be turned OFF only if both S_{1a} and S_{1b} are turned ON. Hence, its gate signal can be represented as:

$$q_2 = \overline{q_{1a} \& q_{1b}} \quad (3)$$

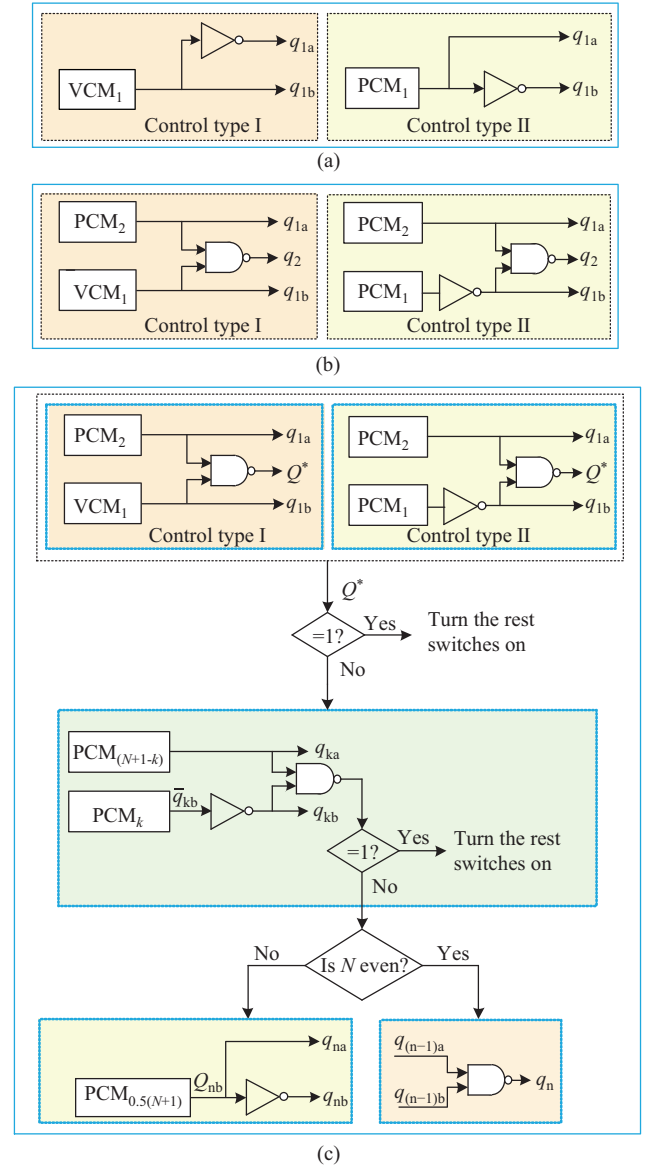


Fig. 4. The control logic block diagram. (a) $N = 1$. (b) $N = 2$. (c) $N \geq 3$.

In this case, bus voltage and power of source V_2 can be fully controlled. In control type II, power of source V_1 and V_2 are preset for tracking control. Thus, the VCM_1 module should be replaced by the PCM_1 with a NOT gate cascaded.

3) When $N > 3$, gate signals can be determined iteratively. The outermost pair of switches S_{1a} and S_{1b} are operated in the same way as case with $N = 2$. If signal q_2 given in (3) is 1, then all the other switches are turned ON because there is already one switch turned OFF; if signal q_2 given in (3) is not 1, then move towards inner to the next pair of switches and operate them in power control mode with PCM. Repeat this until reaching innermost pair of switches S_{na} and S_{nb} if N is odd or S_n if N is even. If N is even, then gate signal for S_n can be directly formed as:

$$q_n = \overline{q_{(n-1)a} \& q_{(n-1)b}} \quad (4)$$

If N is odd, then gate signal for S_{nb} can be generated via corresponding PCM and switch S_{na} can be operated

complementarily. Overall operational logic block diagram is shown in Fig. 4(c) for $N \geq 3$.

C. Steady-state Analysis

1) *Relationship of port voltages*: Assume D_r ($r = 1, 2, \dots, N+1$) represents turned-on duty ratio of switch S_{1b} to S_{1a} , respectively, from bottom to top. Then turned-off duty ratio of each switch is $1 - D_r$. As aforementioned, at any moment, there is one and only one switch turned OFF. Hence, sum of OFF duty ratio of all switches is 1, i.e.,

$$1 - D_1 + 1 - D_2 + \dots + 1 - D_{N+1} = 1 \quad (5)$$

In a traditional BBDC converter, according to the volt-second balance analysis method, average inductor voltage of a switching interval should be zero at steady state. For the proposed converter, an equivalent BBDC cell is operated to interface the h th ($h = 1, 2, \dots, N$) power source. Thus, in continuous current mode (CCM), average voltage across h -th inductor over a switching interval should also be zero. Based on this principle, there is

$$V_h d_h T + (V_h - V_0)(1 - d_h)T = 0 \quad (6)$$

where d_h represents duty ratio of lower common switch of buck/boost cell in respect to source V_h , which can be expressed as:

$$d_h = \sum_{i=h+1}^{N+1} (1 - D_i) \quad (7)$$

As discussed in the previous subsection, if source V_1 is dedicated to regulating DC-bus voltage, then DC-bus voltage V_0 can be represented by:

$$V_0 = \frac{1}{1 - D_1} V_1 \quad (8)$$

According to (6) and (7), relationship between average bus voltage and other source voltages can be expressed as:

$$\begin{cases} V_2 = (1 - d_2)V_0 \\ \vdots \\ V_h = (1 - d_h)V_0 \\ \vdots \\ V_N = (1 - d_N)V_0 \end{cases} \quad (9)$$

Thus, based on (5), (8) and (9), input source voltages are required to meet the following condition

$$V_1 \leq V_2 \leq V_3 \leq \dots \leq V_N \quad (10)$$

This may sound like a very strict constraint, but actually if converter is operated the other way around then it is possible to obtain many low voltage supplies from one voltage source.

2) *Selection of the inductors*: As switching frequency f_s is high enough, inductor current will be piecewise linear. For inductor connected to h -th source, peak-peak current ripple is:

$$\Delta i_h = \frac{V_0 - V_h}{L_h f_s} (1 - d_h) = \frac{d_h (1 - d_h)}{L_h f_s} V_0 \quad (11)$$

According to (11), to obtain a peak-peak current ripple lower than desired value $\Delta i_{h\max}$, inductance should be selected to satisfy the following inequality:

$$L_h \geq \frac{d_h}{\Delta i_{h\max} f_s} (1 - d_h) V_0 \quad (12)$$

3) *Selection of DC-bus Capacitor*: As current in output capacitor is discontinuous a large capacitor is needed to minimize output voltage ripple. According to basic capacitor selection principle of traditional boost converter [36], minimum value of output filter capacitance is given by:

$$C_{0\min} = \frac{D_1 V_0}{V_r R f_s} \quad (13)$$

where V_r is voltage ripple, and R represents output resistance.

D. Maximum Current and Voltage in Each Power Switches

1) Maximum Current Through the Switches

According to operational principle, only one switch is turned-off at any time of a switching cycle. As shown in Fig. 1, if N is odd, upper n switches will reach their maximum current when power switch S_{1b} is off, which can be represented as:

$$I_{\max Sna} = \sum_{k=1}^{N+1-n} |i_{Lk}| \quad (14)$$

Similarly, when power switch S_{1a} is off, lower n switches will reach their maximum current, which can be expressed as:

$$I_{\max Snb} = \sum_{k=n}^N |i_{Lk}| \quad (15)$$

If N is even, maximum current of upper n switches and lower n switches can still be represented by (14) and (15), respectively. However, maximum current of middle switch should be expressed by:

$$I_{\max Sn} = \text{Max} \left(\underbrace{\sum_{k=1}^n |i_{Lk}|}_A, \underbrace{\sum_{k=n+1}^N |i_{Lk}|}_B \right) \quad (16)$$

where A represents current through S_n when S_{1b} is off, and B is current through S_n when S_{1a} is off.

Due to sharing of power switches, current flows in each power switch are related to all inductance current and change according to switching state. As can be concluded in (14)–(16), maximum current of each power switches is different due to connection position. Based on power switches sharing mechanism, it is clear current flows in each switch are different in each switching state. Furthermore, in traditional n pairs of two-quadrant buck/boost DC-DC converters parallel topology (n -BBDC), each BBDC cell is relatively independent so maximum current of power switches in each BBDC cell are only related to its inductance current. Thus, in most cases, current stress of proposed converter would be higher.

2) Maximum Voltage Over the Switches

As only one power switch is off at any time of a switching period, maximum voltage over the switch is equal to bus voltage V_0 . This is the same as traditional n -BBDC topology.

E. Power Losses Analysis

1) Conduction Loss of the Proposed Converter

Based on basic operational principle, the proposed converter can mimic operation of n BBDCs. Each equivalent BBDC would operate in synchronous rectifying mode with the upper and lower power switches conducted complementary. Thus, in synchronous rectify modes, owing to bidirectional conductivity of the MOSFET, freewheeling current will inversely flow in the MOSFET. Thus, conduction loss of each MOSFET is expressed as:

$$P_{\text{cond}} = D_{\text{on}} I_{\text{on}}^2 R_{\text{on}} \quad (17)$$

where P_{cond} is conduction loss of a MOSFET; D_{on} is duty ratio; I_{on} represents average current and R_{on} denotes equivalent resistor of the MOSFET.

Switching loss P_{sw} consists of turned-on loss P_{son} , and turned-off loss P_{soff} .

$$P_{\text{sw}} = P_{\text{son}} + P_{\text{soff}} = \frac{1}{2} V_{\text{ds}} I_{\text{d}} (t_{\text{on}} + t_{\text{off}}) f_{\text{s}} \quad (18)$$

where V_{ds} and I_{d} denotes across voltage and drain current in the MOSFET, respectively; f_{s} represents switch frequency; t_{on} is sum of turn-on rising time and delay time; t_{off} denotes sum of turn-off falling time and delay time.

Based on the operational principle of the proposed converter, when r th power switch is in off state, current in the l th power switch can be represented by:

$$I_{\text{lon}} = \begin{cases} \sum_{k=r}^{l-1} i_{\text{Lk}} & (r < l) \\ 0 & (r = l) \\ \sum_{k=l}^{r-1} i_{\text{Lk}} & (r > l) \end{cases} \quad (19)$$

where $r \in [1, N+1]$ and $l \in [1, N+1]$. S_r and S_l indicate the r th and l th power switch from bottom to top as illustrated in Fig. 1. To be noted here, discharging current is defined as positive current, and vice versa.

Combining (17) and (19), total conduction loss of proposed integrated converter can be obtained as:

$$P_{\text{cond-new}} = \sum_{r=1}^{N+1} \sum_{l=r+1}^{N+1} (1 - D_r) \left(\sum_{k=r}^{l-1} i_{\text{Lk}} \right)^2 R_{\text{on}} + \sum_{r=1}^{N+1} \sum_{l=1}^{r-1} (1 - D_r) \left(\sum_{k=l}^{r-1} i_{\text{Lk}} \right)^2 R_{\text{on}} \quad (20)$$

For traditional n -BBDC converter topology, total conduction loss can be expressed by:

$$P_{\text{cond-traditional}} = \sum_{k=1}^N i_{\text{Lk}}^2 R_{\text{on}} \quad (21)$$

Taken $N = 1$ and $N = 2$ for example, based on (20) and (21), conduction loss difference between the two converters can be represented as:

$$\Delta P_{\text{cond}} = \begin{cases} 0 & (N = 1) \\ [(1 - D_1) i_{\text{L1}}^2 + (1 - D_3) i_{\text{L2}}^2 + 2D_2 i_{\text{L1}} i_{\text{L2}}] R_{\text{on}} & (N = 2) \end{cases} \quad (22)$$

When $N = 1$, the two converter topologies are the same so their total conduction losses are equal. However, as can be seen in (22), when $N = 2$, conduction loss difference is determined by charging or discharging operation modes of power source. If $\Delta P_{\text{cond}} = 0$, there is

$$(1 - D_1) i_{\text{L1}}^2 + (1 - D_3) i_{\text{L2}}^2 + 2D_2 i_{\text{L1}} i_{\text{L2}} = 0 \quad (23)$$

To deem (23) as a quadratic equation of i_{L1} , solutions of the equation are

$$i_{\text{L1}-1} = \lambda_1 i_{\text{L2}} \text{ and } i_{\text{L1}-2} = \lambda_2 i_{\text{L2}} \quad (24)$$

where

$$\begin{cases} \lambda_1 = \frac{-D_2 + \sqrt{D_2^2 - (1 - D_1)(1 - D_3)}}{(1 - D_1)} \\ \lambda_2 = \frac{-D_2 - \sqrt{D_2^2 - (1 - D_1)(1 - D_3)}}{(1 - D_1)} \end{cases} \quad (25)$$

It can be noted that $\lambda_2 < \lambda_1 < 0$.

As shown in Fig. 5, relationship of two sources currents can be plotted as two boundary lines. In the two boundary lines, conduction losses of two converters are equal. In the region between two intersecting boundary lines (region I in the figure), conducting loss of the proposed integrated converter would be less than traditional 2-BBDC converter. However, in other regions, conduction loss in the proposed topology is higher. This would be a limitation of proposed converter when two power sources are operating in charge or discharge modes at the same time. The main reason for increase of conduction loss in this converter is there are several power switches shared during operation of converter.

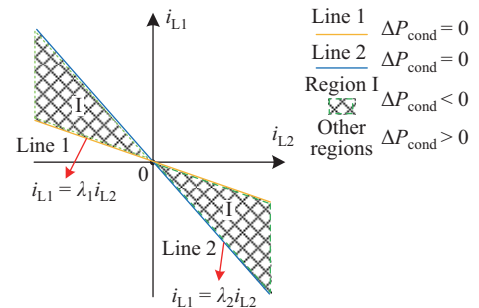


Fig. 5. Conduction loss comparison result.

2) Switching Loss of the Proposed Integrated Converter

Based on the operational principle of the proposed integrated converter, all power switches between the S_{1b} and S_{1a} are shared. Switching frequencies of these shared power switches are twice S_{1b} and S_{1a} . Thus, switching losses in each switch are expressed by

$$\begin{cases} P_{sw-S_1} = \frac{1}{2}V_0(t_{on} + t_{off})f_s|i_{L1}| \\ P_{sw-S_r} = \frac{1}{2}V_0(t_{on} + t_{off})f_s[|i_{Lr}| + |i_{L(r-1)}|] \\ P_{sw-S_{N+1}} = \frac{1}{2}V_0(t_{on} + t_{off})f_s|i_{LN}| \end{cases} \quad (26)$$

Thus, total switching loss in the proposed integrated converter can be obtained as:

$$\begin{aligned} P_{sw} &= \frac{1}{2}V_0(t_{on} + t_{off})f_s \\ &\quad \left\{ \sum_{r=2}^N [|i_{Lr}| + |i_{L(r-1)}|] + |i_{L1}| + |i_{LN}| \right\} \\ &= V_0(t_{on} + t_{off})f_s \sum_{r=1}^N |i_{Lr}| \end{aligned} \quad (27)$$

For traditional n -BBDC converter, total switching loss can be represented by

$$P_{sw-nBBDC} = V_0(t_{on} + t_{off})f_s \sum_{r=1}^N |i_{Lr}| \quad (28)$$

It is clear overall switching losses in the proposed converter and traditional n -BBDC converter are equal.

F. A Summary of the Comparison Between the Proposed Converter with the Traditional N -BBDC

The proposed integrated converter can mimic operation of N buck/boost bidirectional DC-DC converters parallel connected structure (n -BBDC). A summary of comparison of two converter topologies are as follows:

- In topology, to interface N chargeable/dischargeable power sources, only $N + 1$ power switches and N inductors are required. No other additional power devices are needed. However, in traditional n -BBDC structure, $2N$ power switches are needed. This would be the main advantage of the proposed converter as it has more compact structure and can ensure modular design.
- Operational frequencies of shared power switches except S_{1b} and S_{1a} are twice higher. Thus, total switching loss in the proposed converter and traditional n -BBDC are equal.
- Due to switching losses in the two topologies being equal, efficiency is determined by conduction losses. As

analyzed in part E, overall conduction loss would be varied according to charging/discharging conditions of each power source. To be noted here, when all power sources are charged or discharged at the same time, overall conduction loss in the proposed converter would be higher. But in some cases, with partial power sources charging and partial power sources discharging, conduction loss of the proposed converter can be lower. The same is true of efficiency comparisons.

- Voltage of power sources should meet the condition as represented in (10), which is a possible restriction on selection of power sources. But as the proposed converter can ensure bidirectional power flow in all ports, it is also possible to output many low voltage supplies from one voltage source.

III. CASE STUDY WITH $N = 2$

A. Converter Topology When $N = 2$

When $N = 1$, the proposed converter is exactly a traditional buck/boost DC-DC converter widely used in many industrial applications.

When $N = 2$, as shown in Fig. 6, three power switches are connected in series to interface two input bidirectional power sources. As compared with case $N = 1$, only one additional commonly used power switch is integrated. According to (14)–(16), as compared with cases with $N > 3$, the three switches topology ($N = 2$) is integrated topology with lowest maximum current in each switch. Therefore, case $N = 2$ has much better application prospects. Thus, to verify validity of the proposed integrated topology and its control strategies, topology with $N = 2$ is used as a case study in this paper. To be noted here, loads of converter can be flexibly selected. Typical DC load types can be resistor, LED, DC-DC converter-based DC-load systems, inverter-based motor drive systems and bidirectional power source or energy storage systems.

B. Operational Modes Analysis

Without loss of generality, to analyze operational modes of dual-input-based DC-DC converter, load type 2 as shown in Fig. 6 is used as an example. In case of load type 2, as all

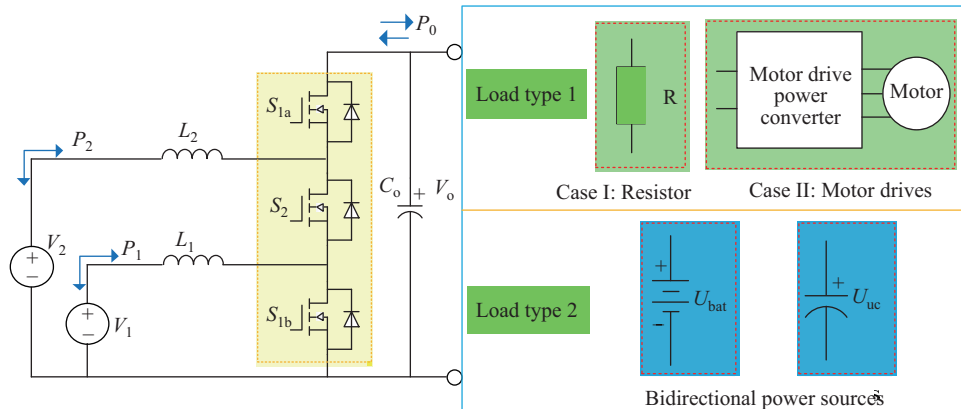
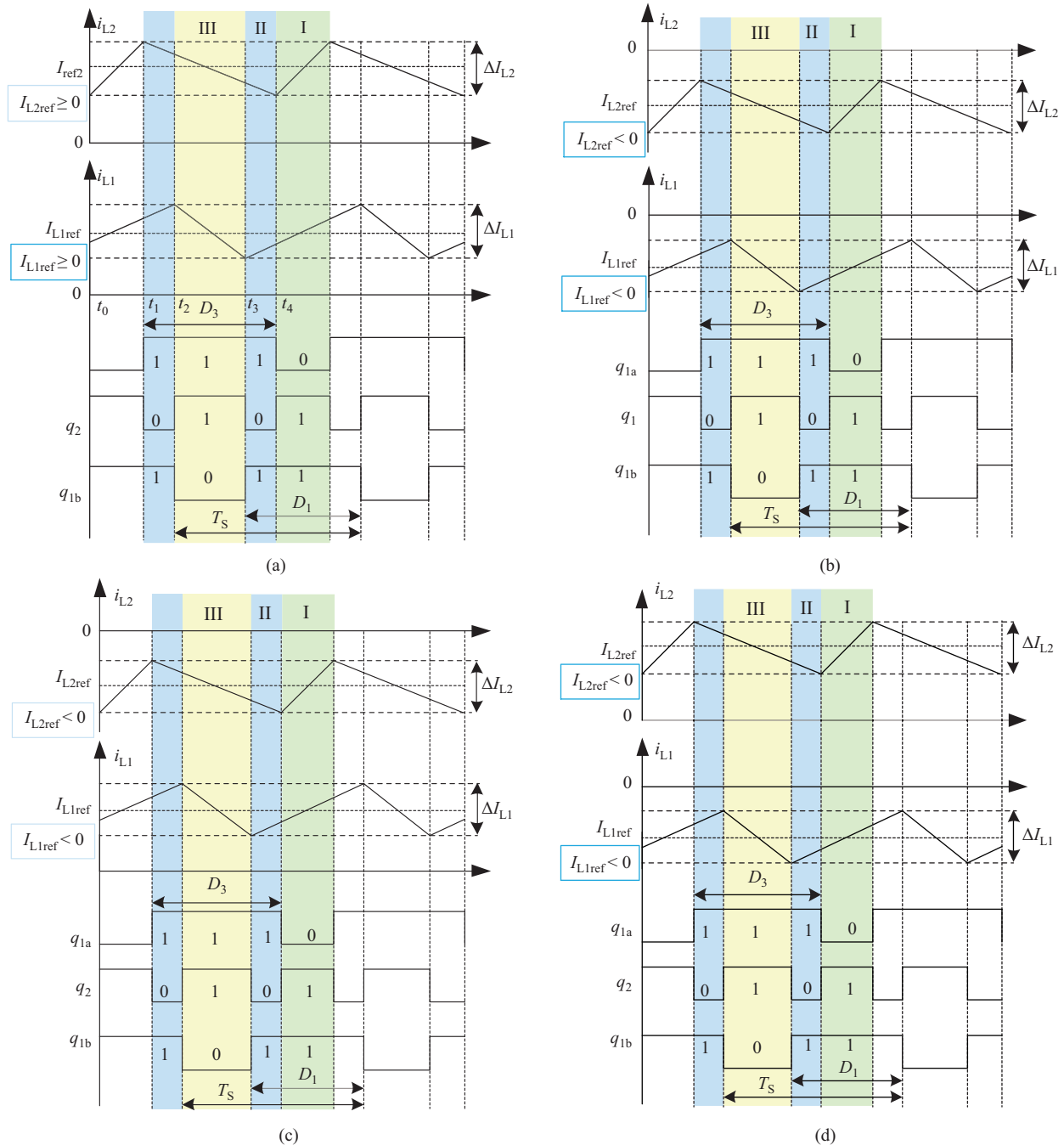


Fig. 6. The topology of the converter with $N = 2$.



Note: I_{L1ref} and I_{L2ref} are the reference current of the two inductance i_{L1} and i_{L2} , q_{1a} , q_2 , and q_{1b} are the switching signal of each power switch.

Fig. 7. Principle diagram of the six operational modes. (a) For mode I ($P_1 \geq 0$, $P_2 \geq 0$, $P_0 \leq 0$). (b) For mode II ($P_1 < 0$, $P_2 < 0$, $P_0 > 0$). (c) For mode III ($P_1 \geq 0$, $P_2 < 0$, $P_0 \leq 0$) and mode IV ($P_1 \geq 0$, $P_2 < 0$, $P_0 > 0$). (d) For mode V ($P_1 < 0$, $P_2 \geq 0$, $P_0 \leq 0$) and mode VI ($P_1 < 0$, $P_2 \geq 0$, $P_0 > 0$).

three ports of converter should be bidirectional, six power flow modes would be included.

Inductance current waveforms and switching signals under the six operational modes are illustrated in Fig. 7. As shown in the figure, in any possible operational modes, only three switching states with 110, 101, 011 switching logics may exist. With these switching logics, any two switches and third one can be controlled in complement. Thus, it is possible to mimic operation of two traditional BBDCs. As illustrated in Fig. 7, energy flows in all three ports can be bidirectional. In addition,

as can be seen in all of six operational modes, owing to sharing of switch S_2 , its switching frequency is twice that in the other two switches.

C. Control Strategies

Considering load types, two control strategies are developed according to basic operational principle as discussed in the previous section. In this paper, resistor, switched reluctance motor (SRM) drive and battery are used as examples to represent different types of loads.

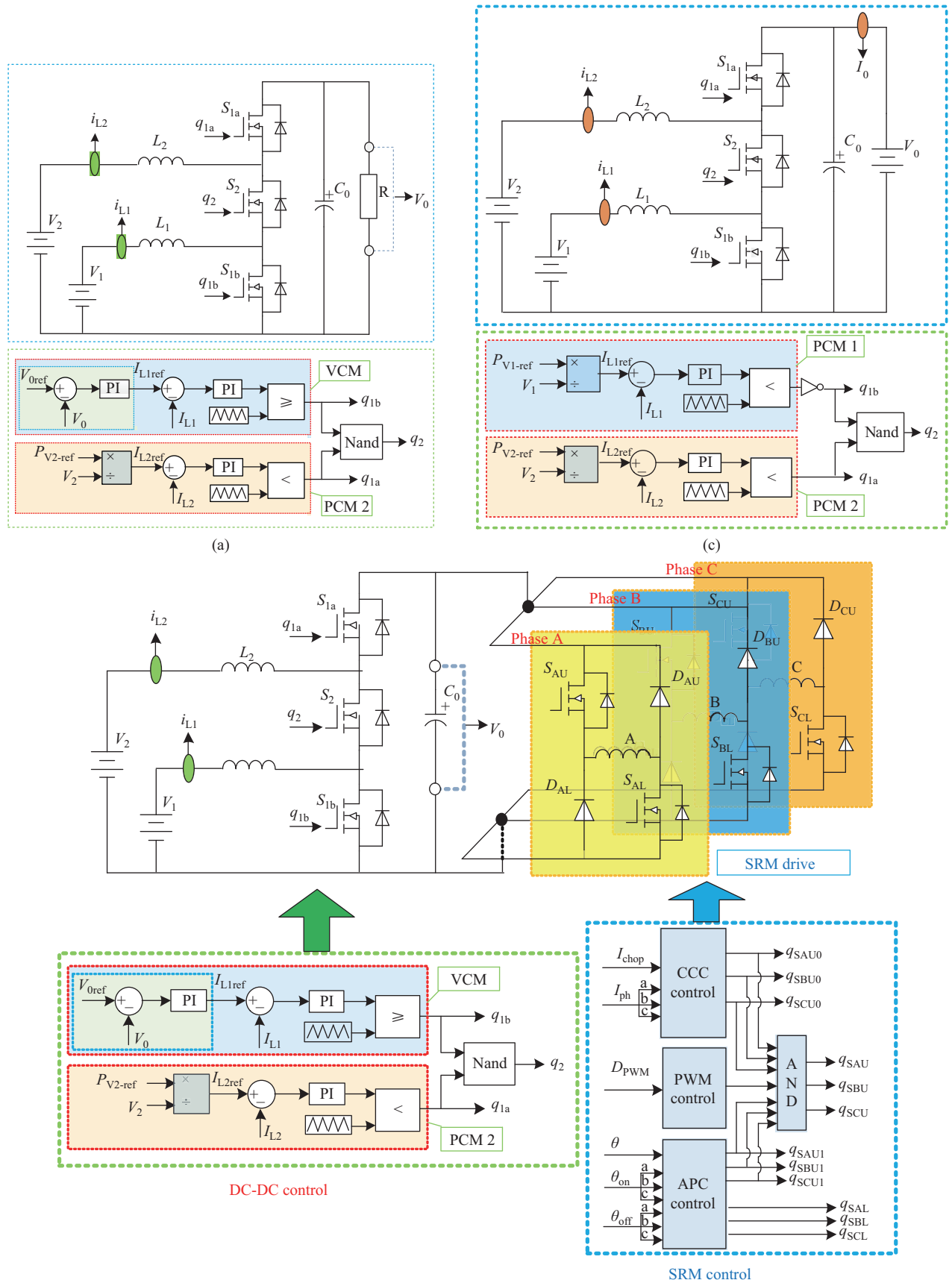


Fig. 8. Control block diagram of the converter under different load cases. (a) Load type 1 (Case I: resistor). (b) Load type 1 (Case II: SRM based motor drives). (c) Load type 2 (Battery).

1) *Load type 1 (Case I: resistor)*: According to general control strategies as illustrated in Fig. 3, VCM₁ control module is utilized to generate PWM signals for power switch S_{1b} . PCM₂ control module with preset power reference is used for controlling power switch S_{1a} . Then, gate signal in shared switch S_2 can be derived by $Nand$ logic of the other two switching signals. As shown in Fig. 8(a), bus voltage can be controlled by power source V_1 through the VCM₁ control module, and power flow between input and output can also be handled by power source V_1 automatically.

2) *Load type 1 (Case II: SRM based motor drive)*: In this case, resistor load as shown in Fig. 8(a) is replaced with a three-phase asymmetric half-bridge converter (AHBC) based SRM drive. As presented in Fig. 8(b), control of dual-source based DC-DC converter part is the same as case with resistor load. DC-bus voltage in AHBC can be controlled to maintain constant value to support power for the SRM drive. Control of DC-DC converter and SRM drive are independent. Generally, all basic control algorithms for SRM drives such as current chopping control (CCC), angle position control (APC), and pulse width modulation control (PWM) can be adopted here. In this paper, hybrid APC, CCC and PWM control algorithm is utilized as an example. As shown in Fig. 8(b), based on APC control strategy, by comparing rotor position with switching angles θ_{on} and θ_{off} in each phase, conduction regions of each phase can be selected. In conduction region, upper power switch of each phase leg of the AHBC is regulated by current chopping signal and PWM signal, and thus amplitude of phase currents can be restricted, and rotor speed can be adjusted.

3) *Load type 2 (battery as an example)*: As illustrated in Fig. 8(c), as DC-bus voltage is automatically restricted by load battery, VCM₁ module can be replaced with PCM₁ module. It should be noted switching signal S_{1b} should be complementary signal of PCM₁ output, and switching signals of S_{1a} and S_2 can be obtained with similar ways as load type 1. In this case, two PCM modules are used for managing power flows of the two sources, and thus power difference between the two sources can be handled by the battery of load side.

IV. EXPERIMENTAL VERIFICATION

A. Introduction of the Test-bed

To verify validity of the proposed converter topology and its control strategies, topology with $N = 2$ is used as a case study. A prototype with two input power sources ($N = 2$), and with different loads such as resistor load (load type 1, Case I), SRM based motor drive (load type 1, Case II) and battery (load type 2) are developed for testing. Picture of test-bed is shown in Fig. 9 and basic specifications of test-bed is included in Table II. In experiments, a DSP28335 based controller is used for implementing overall control algorithms.

B. Controller Design and Analysis

As aforementioned, equivalent BBDC converters can be controlled through basic VCM and PCM control modules. Actually, the VCM is a voltage-current cascaded control loop and the PCM is a single current control loop. Thus, controller design process is the same as traditional BBDC converter,

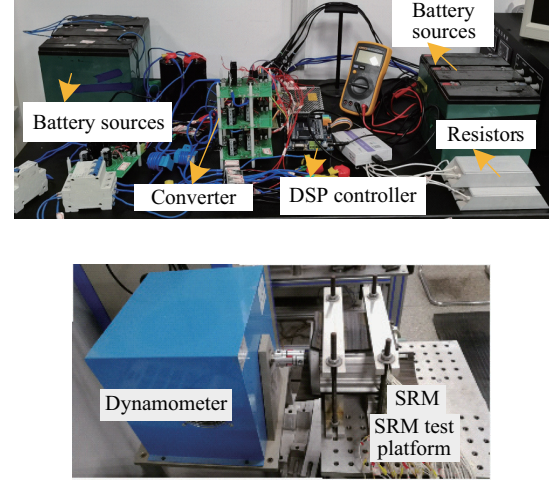


Fig. 9. The picture of the test-bed.

TABLE II
SPECIFICATION OF THE TEST-BED

Parameter	Value
Battery bank (V_1)	12 V, 20 AH
Battery bank (V_2)	2×12 V, 20 AH
Resistor load (Ω) (Load type 1, case I)	30 Ω
SRM drive (Load type 1, case II)	12/8 structure, 0.5 kW
Battery bank (V_0) (Load type 2)	3×12 V, 20 AH
Inductor (L_1 and L_2)	3 mH
Switching frequency (f_s)	20 kHz
Capacitor C_0	1000 μ F

which can be analyzed with small signal model and bode diagram. Without losing generality, controller design for the case with load type 1 is analyzed as an example. For load type 2, two PCMs can be designed in the similar way. Take load type 1 for an example, the VCM controller design process is discussed as follows.

In inner current loop, transfer function of duty ratio to inductance current can be represented by:

$$G_{id}(s) = \frac{\hat{i}_L(t)}{\hat{d}(t)} = \frac{V_0 C s + \frac{2V_0}{R_L}}{L C s^2 + \frac{L}{R_L} s + (1 - d_h)^2} \quad (29)$$

For outer voltage loop, transfer function of inductance current to output voltage is represented by:

$$G_{vi}(s) = \frac{\hat{v}_o(t)}{\hat{i}_L(t)} = \frac{R_L(1 - d_h)^2 - sL}{C R_L(1 - d_h)s + 2(1 - d_h)} \quad (30)$$

where $\hat{d}(t)$, $\hat{v}_s(t)$, $\hat{i}_L(t)$ and $\hat{v}_o(t)$ represent AC small signal component of duty ratio, input voltage, inductance current and output voltage, respectively. d_h represents duty ratio of lower common switch in buck/boost converter in respect to source V_h . Transfer functions of inner PI regulator can be expressed as:

$$G_{pi-in}(s) = k_{p-in} + \frac{k_{i-in}}{s} \quad (31)$$

and outer PI regulator can be expressed as:

$$G_{pi-out}(s) = k_{p-out} + \frac{k_{i-out}}{s} \quad (32)$$

where k_{p-in} , k_{i-in} , k_{p-out} , and k_{i-out} are proportional integral (PI) coefficients of inner and outer PI regulators, respectively.

Based on (1)–(4), open loop transfer function of inner current loop $G_{i_loop}(s)$ can be expressed as:

$$G_{i_loop}(s) = G_{PI-in}(s)G_{id}(s) \quad (33)$$

and open loop transfer function in outer voltage loop $G_{v_loop}(s)$ can be represented by:

$$G_{v_loop}(s) = G_{pi-out}(s)G_{vi}(s) \frac{G_{pi-in}(s)G_{id}(s)}{1 + G_{i_loop}(s)} \quad (34)$$

For power source V_1 , VCM control module consists an inner current loop and an outer voltage loop. The bode diagram of transfer function in the two control loops are shown in Fig. 10. As shown in Fig. 10(a), in inner current controller, cut off frequency is 2 kHz, amplitude margin is infinite and phase margin is 87 degree, which indicates control system is stable. As shown in Fig. 10(b), outer voltage controller has a 40 Hz cut-off frequency, 16.3 dB amplitude margin and 40.7 degree phase margin, which indicates system is also stable. For power source V_2 , PCM_2 can be deemed as a single current control loop with a PI regulator. The bode diagram of transfer function of the PCM_2 is shown in Fig. 11. Similar to that in inner current controller of the VCM, cut off frequency is 2 kHz, amplitude margin is infinite, and phase margin is 87 degree, thus system is stable.

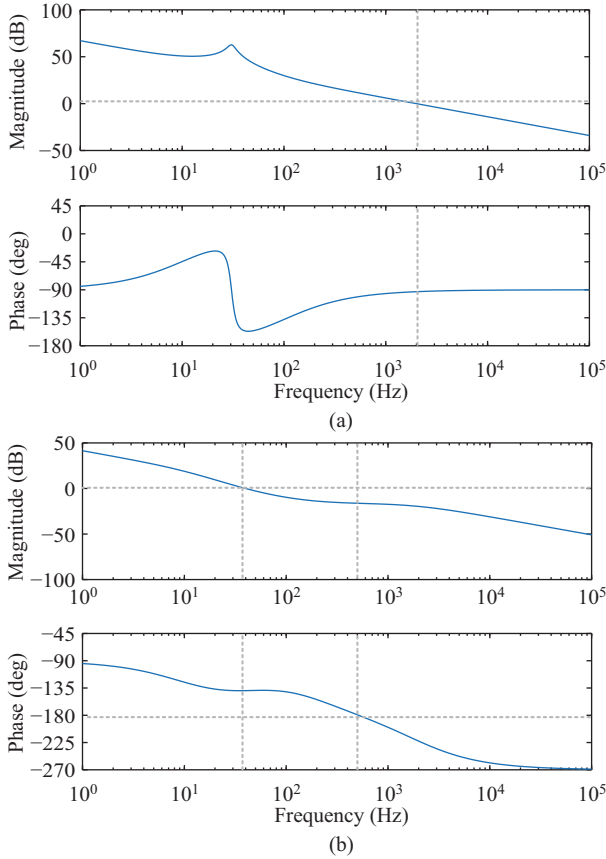


Fig. 10. The Bode diagram of the transfer function of inner and outer control loop of the VCM. (a) Inner current loop of the VCM. (b) Outer voltage loop of the VCM.

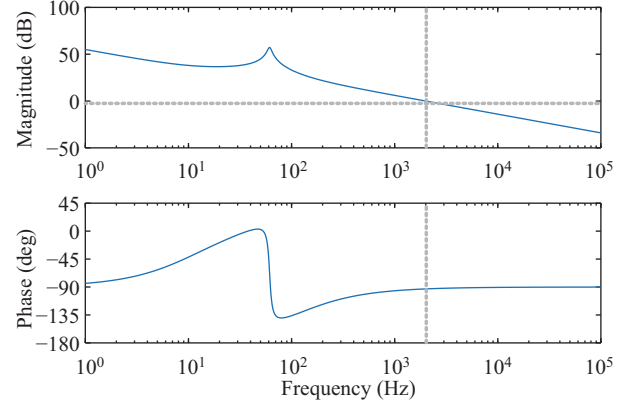


Fig. 11. The bode diagram of the transfer function of the PCM_2 .

C. Experimental Results

Based on the test-bed, different testing scenarios are preset for experiments, which is arranged in Table III. Detailed analysis of experimental results under different load cases is discussed as follows.

TABLE III
DIFFERENT TESTING SCENARIOS IN EXPERIMENTS

Load type	Operation mode	Parameters
Load type 1, Case I Resistor load	Model I	$I_{L2ref} = 1 \text{ A}$, $V_0 = 36 \text{ V}$
	Model III	$I_{L2ref} = -0.5 \text{ A}$, $V_0 = 36 \text{ V}$
	Model V	$I_{L2ref} = 2.5 \text{ A}$, $V_0 = 36 \text{ V}$
Load type 1, Case II SRM drive	Model I	$I_{L2ref} = 0.5 \text{ A}$, $V_0 = 36 \text{ V}$
	Model III	$I_{L2ref} = -0.5 \text{ A}$, $V_0 = 36 \text{ V}$
	Model V	$I_{L2ref} = 2 \text{ A}$, $V_0 = 36 \text{ V}$
Load type 2 Battery bank	Model I	$I_{L1ref} = 2.5 \text{ A}$, $I_{L2ref} = 1 \text{ A}$
	Model II	$I_{L1ref} = -2.5 \text{ A}$, $I_{L2ref} = -2 \text{ A}$
	Model III	$I_{L1ref} = 2.5 \text{ A}$, $I_{L2ref} = -0.5 \text{ A}$
	Model IV	$I_{L1ref} = 2.5 \text{ A}$, $I_{L2ref} = -2 \text{ A}$
	Model V	$i_{L1} = -2.5 \text{ A}$, $I_{L2ref} = 2 \text{ A}$
	Model VI	$I_{L1ref} = -2.5 \text{ A}$, $I_{L2ref} = 0.5 \text{ A}$

For load type 1 case I, control algorithm as illustrated in Fig. 8(a) is utilized. As battery bank voltage has little variation, current reference I_{L2ref} of the PCM control module can be preset directly to mimic a fixed given power reference. For verification, three possible operation modes such as Mode I, III, and V are tested with I_{L2ref} preset as 1 A, 2.5 A, and -0.5 A , respectively.

As shown in Fig. 12, whether current reference I_{L2ref} is positive, or negative, bus voltage can be flexibly controlled to track given voltage reference 36 V as battery bank V_1 can be charged or discharged to overcome power differences between battery tank V_2 and resistor load.

For load type 1 case II, according to control principle as illustrated in Fig. 8(b), bus voltage V_0 can be maintained to support power for the AHBC based SRM drive system. In test experiments, DC-bus voltage reference is preset at 36 V, a 5kHz switching frequency with fixed PWM duty ratio $D_{PWM} = 0.4$ and a chopping current reference $I_{chop} = 8 \text{ A}$ is applied in the AHBC for SRM control.

As illustrated in Fig. 13(a)–(c), once I_{L2ref} preset as 0.5 A, -0.5 A , and 2 A, respectively, the SRM can operate under constant speed 2500 r/min, and input/output power of lower

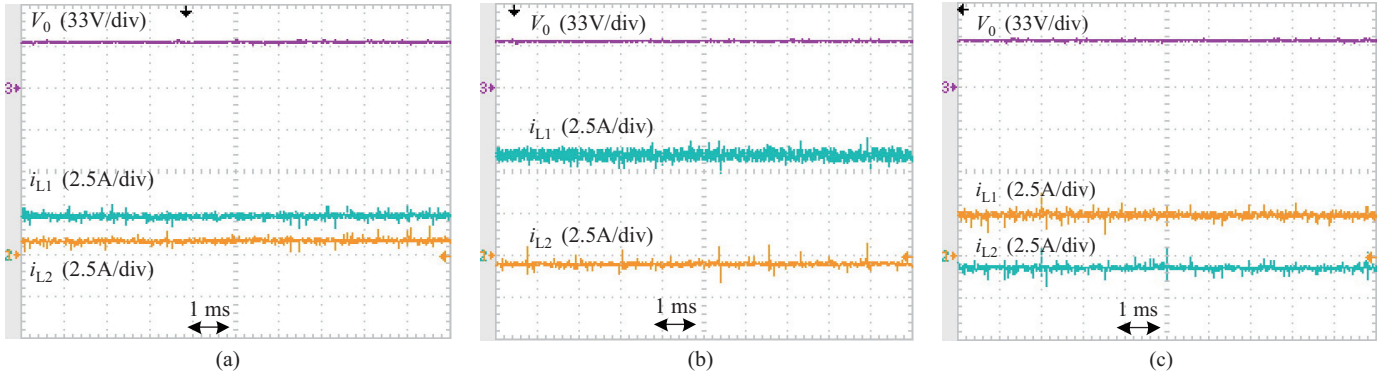


Fig. 12. The power flow modes in resistor load case (load type 1, Case I). (a) For mode I ($I_{L2ref} = 1$ A, $V_0 = 36$ V). (b) For mode III ($I_{L2ref} = -0.5$ A, $V_0 = 36$ V). (c) For mode V ($I_{L2ref} = 2.5$ A, $V_0 = 36$ V).

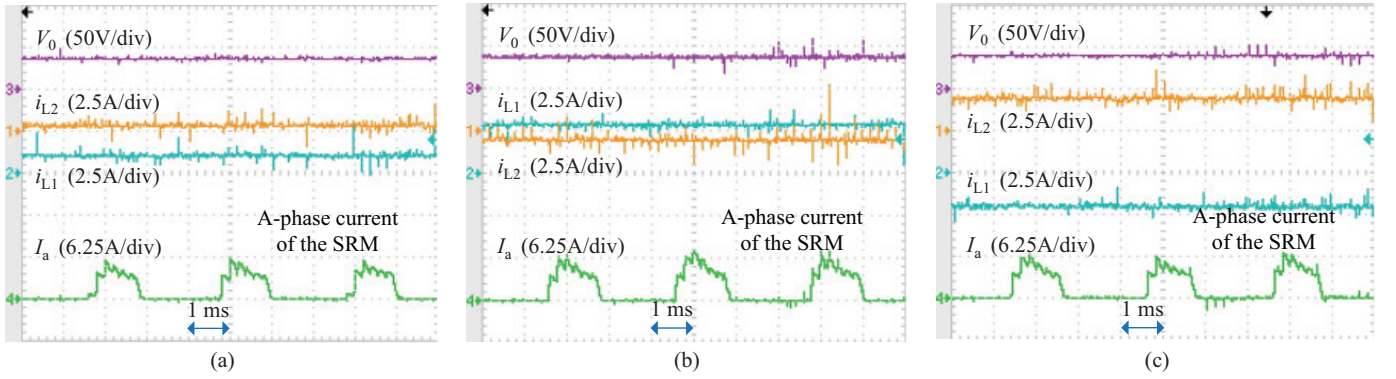


Fig. 13. The power flow modes with SRM drive load (load type 1, Case II). (a) For mode I ($I_{L2ref} = 0.5$ A, $V_0 = 36$ V). (b) For mode III ($I_{L2ref} = -0.5$ A, $V_0 = 36$ V). (c) For mode V ($I_{L2ref} = 2$ A, $V_0 = 36$ V).

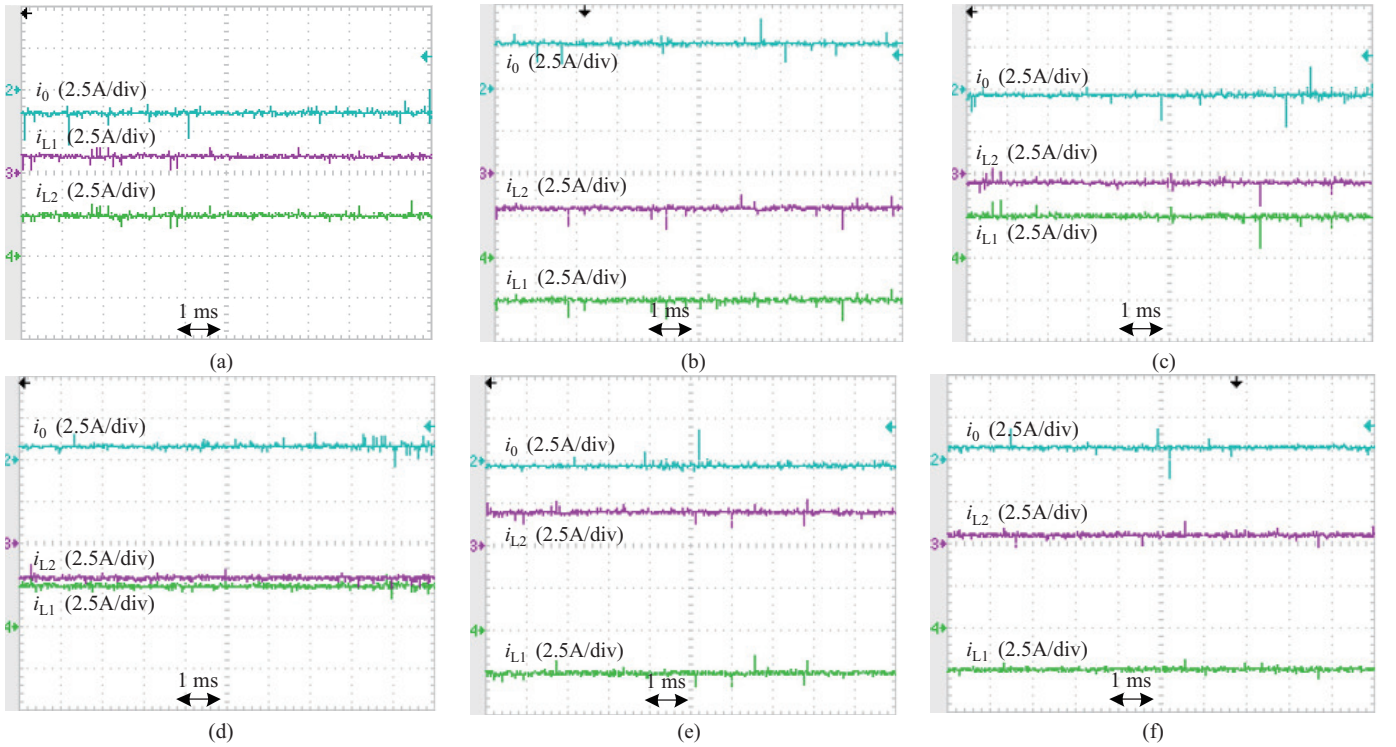


Fig. 14. Six power flow modes in load type 2. (a) For mode I ($I_{L1ref} = 2.5$ A, $I_{L2ref} = 1$ A). (b) For mode II ($I_{L1ref} = -2.5$ A, $I_{L2ref} = -2$ A). (c) For mode III ($I_{L1ref} = 2.5$ A, $I_{L2ref} = -0.5$ A). (d) For mode IV ($I_{L1ref} = 2.5$ A, $I_{L2ref} = -2$ A). (e) For mode V ($I_{L1ref} = -2.5$ A, $I_{L2ref} = 2$ A). (f) For mode VI ($I_{L1ref} = -2.5$ A, $I_{L2ref} = 0.5$ A).

source V_1 can be adjusted freely according to load cases. It is also clear power flow of the two source ports can be bidirectional.

For load type 2, control algorithm as shown in Fig. 8(c) is utilized. As variation in the two input battery bank voltages is low, it is possible to mimic the six operational modes as shown in Fig. 7 by presetting current references of the two input inductors.

As shown in Fig. 14, two inductors current can track references well with basic control algorithm in Fig. 8(c). Once input currents are regulated into references, input powers of two input battery banks are nearly determined, and power difference between input and output should be provided or absorbed by battery bank attached in load side. Furthermore, as illustrated in Fig. 14, all battery banks in input side and output side can be charged or discharged once reference current of two inductors change, which verifies basic characteristics all input/output ports of proposed multi-input converter can be bidirectional.

Dynamic operation results of the six modes as listed in Table III can be seen in Fig. 15. As shown in this figure, even though power references of the two sources are changed dynamically, converter can still be operated stably.

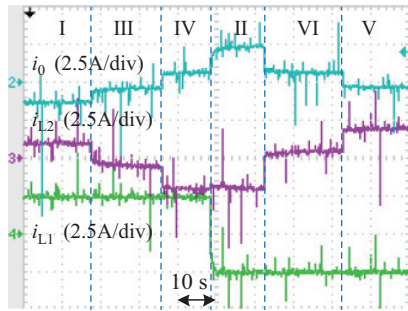


Fig. 15. Dynamic operation of the six power flow modes in load type 2.

V. CONCLUSION

A general multi-input bidirectional DC-DC converter topology for hybrid energy storage systems is developed in this paper. Control logic and operational principle are analyzed systematically. This converter is attractive as it only requires $N + 1$ power switches to interface N bidirectional power sources. Due to its compact structure, modular design and flexible control capability, converter is possible to be applied in hybrid energy storage systems. However, owing to sharing of power switches in operation, current flowing in each power switch is related to all inductance current and changes according to the switching state. Thus, maximum current in each switch is different due to connection position. Compared with traditional n -BBDC structures, current stress of proposed converter would be higher. Cases with two sources ($N = 2$) can ensure lowest maximum current in each switch as compared with cases $N > 2$. Thus, $N = 2$ topology can be selected as a simplistic integrated converter module, which is also possible to combine with BBDC module to construct series connected or parallel connected multi-input integrated

converters flexibly for needs of different applications. In this paper, $N = 2$ topology is tested as a general study case. Experimental results under different typical load types such as resistor load, SRM drive based load and battery are provided for verification, which show bus voltage and power flow in all ports can be flexible controlled via the proposed control strategies.

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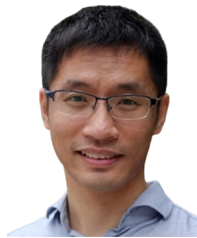
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